CY2SSTV8575

Differential Clock Buffer/Driver

Features

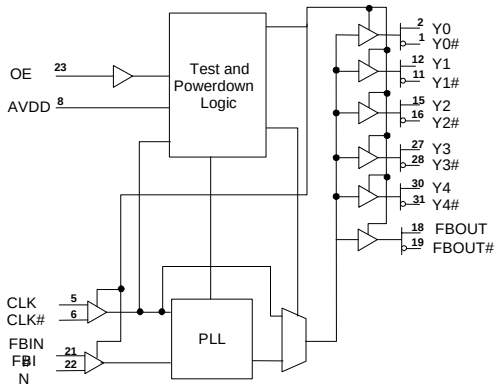
- **Operating frequency: 60 MHz to 170 MHz**
- **Supports 266-MHz DDR SDRAM**
- **5 differential outputs from 1 differential input**
- **Spread Spectrum compatible**
- **Low jitter (cycle-to-cycle): < 75**
- **Very low skew: < 100 ps**
- **Power Management Control input**
- **High-impedance outputs when input clock < 20 MHz**
- **2.5V operation**
- **32-pin TQFP JEDEC MS-026 C**

Description

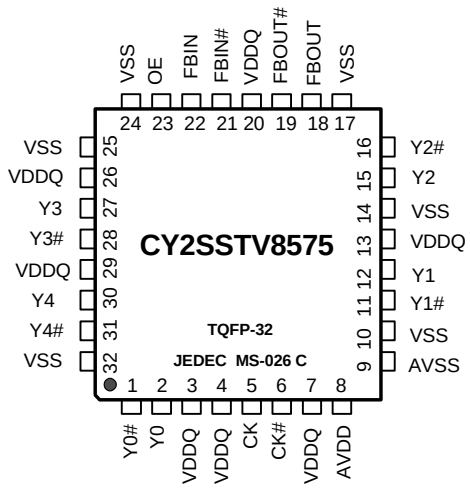
The CY2SSTV8575 is a high-performance, low-skew, low jitter zero-delay buffer designed to distribute differential clocks in high-speed applications. The CY2SSTV8575 generates five differential pair clock outputs from one differential pair clock input. In addition, the CY2SSTV8575 features differential feedback clock outputs and inputs. This allows the CY2SSTV8575 to be used as a zero-delay buffer.

When used as a zero-delay buffer in nested clock trees, the CY2SSTV8575 locks onto the input reference and translates with near zero delay to low-skew outputs.

Block Diagram



Pin Configuration



Pin Description

Pin	Name	I/O	Type	Description
5,6	CLK, CLK#	I	LV Differential Input	**Differential Clock Input**
21	FBIN#	I	Differential Input	**Feedback Clock Input**. Connect to FBOUT# for accessing the PLL.
22	FBIN	I		**Feedback Clock Input**. Connect to FBOUT for accessing the PLL.
2,12,15,27,30	Y(0:4)	O	Differential Outputs	**Clock + Outputs**
1,11,16,28,31	Y(0:4)#	O		**Clock – Outputs**
18	FBOUT	O	Differential Outputs	**Feedback Clock Output**. Connect to FBIN for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
19	FBOUT#	O		**Feedback Clock Output**. Connect to FBIN# for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
23	OE	I		**Output Enable Input**. When OE is set HIGH, all Q and Q# outputs are enabled and switch at the same frequency as CLK. When set LOW, all Q and Q# outputs are disabled (Hi-Z) and the PLL is powered down.
3,4,7,13,20,26, 29	VDDQ		2.5V Nominal	**2.5V Power Supply for Output Clock Buffers**
8	AVDD		2.5V Nominal	**2.5V Power Supply for PLL**. When AVDD is at GND, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (OE = 0), the PLL is powered down.
10,14,17,24,25, 32	VSS		0.0V Ground	**Common Ground**
9	AVSS		0.0V Analog Ground	**Analog Ground**

Table 1. Function Table

INPUTS				OUTPUTS				PLL
AVDD	**OE**	**CLK**	**CLK#**	**Y**	**Y#**	**FBOUT**	**FBOUT#**	
GND	H	L	H	L	H	L	H	BYPASSED/OFF
GND	H	H	L	H	L	H	L	BYPASSED/OFF
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	OFF
2.5V	H	L	H	L	H	L	H	On
2.5V	H	H	L	H	L	H	L	On
2.5V	H	< 20 MHz	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	HI-Z	Off

Power Management Functions

Output enable/disable control of the CY2SSTV8575 allows the user to implement power management schemes into the design. Outputs are three-stated/disabled when OE is asserted low, see *Table 1*. The enabling and disabling of outputs is done in such a manner to eliminate the possibility of the partial “runt” clocks.

Zero Delay Buffer

When used as a zero delay buffer the CY2SSTV8575 will likely be in a nested clock tree application. For these applications the CY2SSTV8575 offers a differential clock input pair as a PLL reference. The CY2SSTV8575 can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback input, FBIN, is connected to the feedback output, FBOUT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with tine input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When AVDD is strapped LOW, the PLL is turned off and bypassed for test purposes.

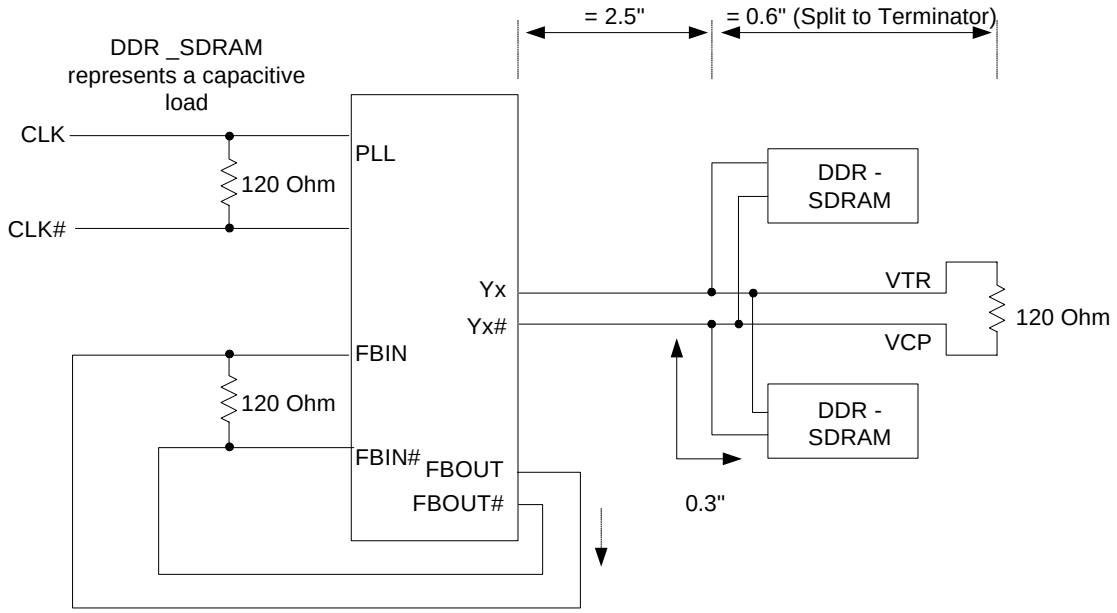


Figure 1. Clock Structure 1[1]

Note:

1. Output load capacitance for 2 DDR-SDRAM loads: 5 pF < CL < 8 pF.

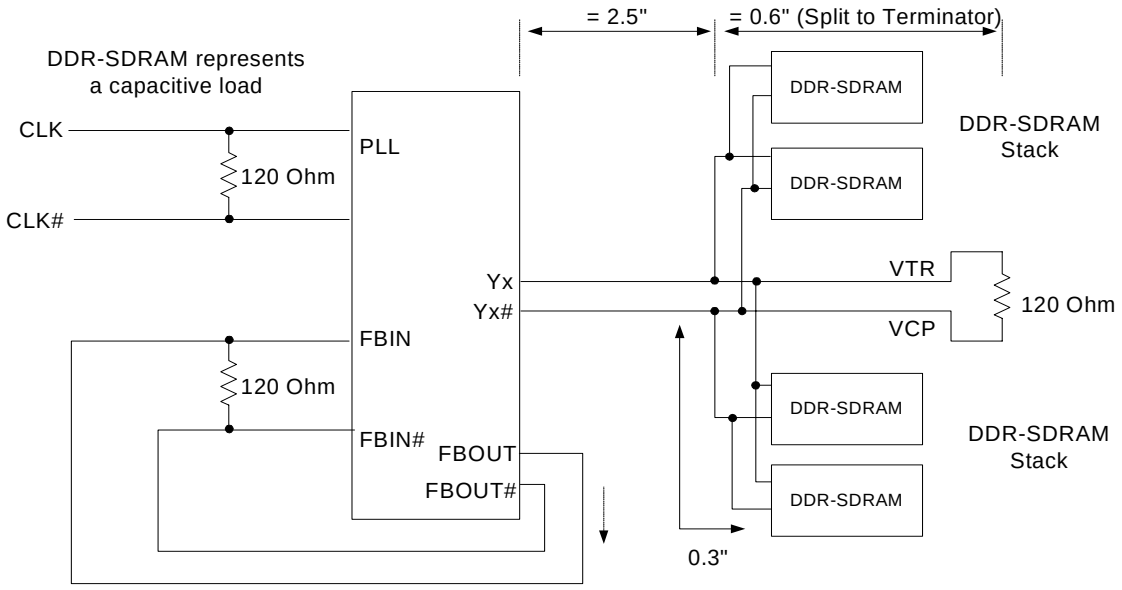


Figure 2. Clock Structure 2[2]

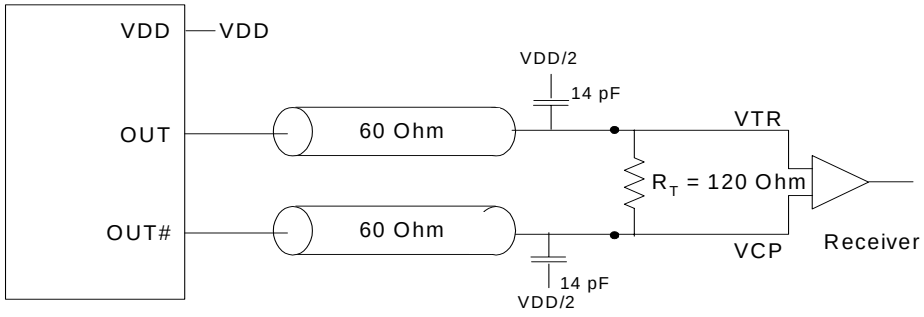


Figure 3. Differential Signal Using Direct Termination Resistor

Governing Agencies

The following agencies provide specifications that apply to the CY2SSTV8575. The agency name and relevant specification is listed below;

Agency Name	Specification
JEDEC	MS - 026-C

Note:
2. Output load capacitance for 4 DDR-SDRAM loads: 10 pF < CL < 16 pF.

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$ (V_{DDQ} Voltage)

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DDQ}).

Parameter	Description	Conditions	Min.	Max.	Unit
V_{dd}	Supply Voltage	Non Functional	–0.3	3.5	VDC
V_{DD}	Operating Voltage	Functional	2.38	2.63	VDC
V_{in}	Input Voltage	Relative to VSS	–0.3	2.63	VDC
V_{out}	Output Voltage	Relative to VSS	–0.3	2.63	VDC
T_s	Temperature, Storage	Non Functional	–65	150	°C
T_a	Temperature, Operating Ambient	Functional	0	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	–	18	°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	–	48	°C/W
ESD_h	ESD Protection (Human Body Model)		–	2K	Volts
FIT	Failure in Time	Manufacturing test	–	10	ppm

DC Parameters ($AV_{DD} = V_{DDO}$ = 2.5 ±5%, Temperature = 0°C to +85°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low[3]	OE	–	–	0.75	V
V_{IH}	Input Voltage, High[3]		1.75	–	–	V
V_{OL}	Output Voltage, Low	V_{DDQ} = 2.375V, I_{OL} = 12 mA	–	–	0.6	V
V_{OH}	Output Voltage, High	V_{DDQ} = 2.375V, I_{OH} = –12 mA	1.7	–	–	V
I_{OL}	Output Low Current	V_{DDQ} = 2.375V, V_{OUT} = 1.2V	26	35	–	mA
I_{OH}	Output High Current	V_{DDQ} = 2.375V, V_{OUT} = 1V	28	–32	–	mA
I_{DDQ}	Dynamic Supply Current[4]	ALL V_{DDQ}, FO = 170 MHz	–	235	300	mA.
I_{PDS}	Power Down Current	OE = 0 or CLK/CLK# < 20 MHz	–	–	100	µA.
C_{in}	Input pin capacitance		–	–	4	pF

Notes:
3. Unused inputs must be held high or low to prevent them from floating.
4. All outputs switching loaded with 16pF in 60Ω environment. See *Figure 3*.

AC Input Parameters (AV_{DD} = VDDQ = 2.5 ±5%, T_A = 0°C to +85°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{in}	Input Frequency	1.25	60	–	170	MHz
D_{TYC}	Input Duty Cycle	AV_{DD}, V_{DD} = 2.5V±0.2V	40	–	60	%

AC Output Parameters (AVDD= VDDQ = 2.5 ±5%, Temperature = 0°C to +85°C)[5,6]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{OR}	Output frequency range	AV_{DD}, V_{DD} = 2.5V±0.2V	60	–	170	MHz
t_{LOCK}	Maximum PLL Lock Time	AV_{DD}, V_{DD} = 2.5V±0.2V	–	–	100	µS
D_{TYC}	Duty Cycle[7]	60 MHz to 100 MHz	49.5	50	50.5	%
		101 MHz to 170 MHz	49	–	51	%
T_R	Rise Time	20% to 80% of V_{OD}	1	–	2	V/ns
T_F	Fall Time	20% to 80% of V_{OD}	1	–	2	V/ns
t_{SKEW}	Any Output to Any Output Skew[9]	All outputs equally loaded	–	–	100	ps
T_{PLH}	Propagation Delay (Low to High)	CLK to Y	1.5	3.5	6	ns
T_{PHL}	Propagation Delay (High to Low)	CLK to Y	1.5	3.5	6	ns
T_{ODIS}	Output Disable Time[8]	All outputs	–	3	–	ns
T_{OENB}	Output Enable Time[8]	All outputs	–	3	–	ns
$T_{JIT(CC)}$	Cycle to Cycle Jitter	All outputs @ 66 MHz	–100	–	–100	ps
T_{PHASE}	Phase Error		–150	–	150	ps
$T_{JIT(PHASE)}$	Phase Error Jitter	All outputs @ 66 MHz	–50	–	50	ps

Notes:

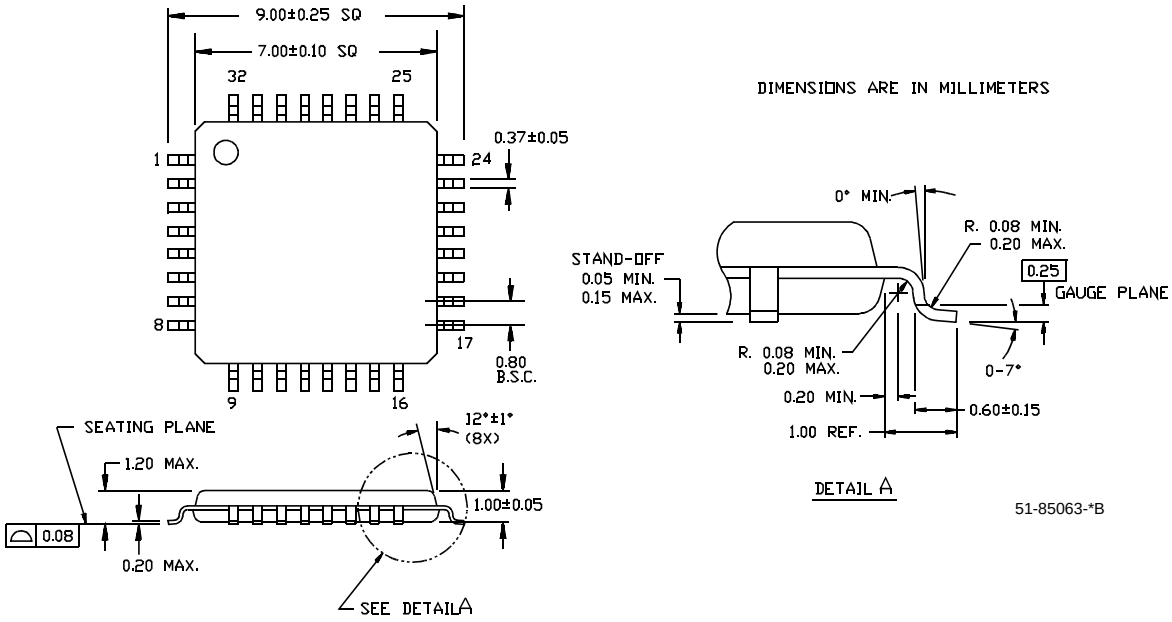
5. Parameters are guaranteed by design and characterization. Not 100% tested in production.
6. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 50 kHz with a down spread of –0.5%.
7. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/t_C, where the cycle time (t_C) decreases as the frequency goes up.
8. Refers to transition of non-inverting output.
9. All differential input and output terminals are terminated with 120Ω/16 pF as shown in *Figure 2*.

Ordering Information

Part Number	Package Type	Product Flow
CY2SSTV8575AC	32-pin TQFP	Commercial, 0° to 85°C
CY2SSTV8575ACT	32-pin TQFP -Tape & Reel	Commercial, 0° to 85°C

Package Drawing and Dimension

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm A32



Document History Page

Document Title: CY2SSTV8575 Differential Clock Buffer/Driver Document #: 38-07458				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	120711	10/31/02	RGL	New Data Sheet